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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,286	07/12/2000	Hiroshi Tanabe	NECK 17.552	2375

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EXAMINER

KIELIN, ERIK J

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 04/17/2003

24

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/614,286

Applicant(s)

TANABE, HIROSHI

Examiner

Erik Kielin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 February 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,4,6-8 and 10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,6-8 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 22.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This action responds to the IDS filed 13 January 2003 (Paper No. 22) and the Amendment filed 7 February 2003 (Paper No. 23).

Information Disclosure Statement

Examiner notes that what appears to be a translation of a rejection of the instant claims by some other patent office, perhaps the Japanese Patent Office has been included along with the Japanese Patent Publication 06-163590, cited in the action, but this reference is not listed in the IDS and, accordingly, has not been considered.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 3, 4, 6, and 10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The limitations of claims 2 and 9 were incorporated into independent claims 1 and 7, respectively. However, the specification indicates that the limitations of claims 2 and 9 are conflicting with the limitations of claims 3 and 10, respectively, because the limitations are referred to as alternatives. (See instant specification at paragraph bridging pp. 21-22.)

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Accordingly, there is no teaching in the instant specification to combine the limitations of claims 2 and 3 or 9 and 10, which has been done by the most recent amendment.

Moreover, independent claims 1 and 7 require the alignment mark to be formed on the substrate prior to step (a), yet claims 3 and 10 contradictorily indicate that the alignment mark is formed on the substrate by the irradiation step in step (d).

Moreover, Applicant's specification does not provide support for forming an alignment mark on the substrate in step (a) to be used for positioning, and then also forming a different alignment mark on the substrate in step (d) to be used for positioning.

Claims 4 and 6 are rejected for depending from claim 3.

For the purposes of patentability, the claims will be interpreted as best understood by Examiner.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 4, 6, and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 10 use the term "alignment mark" to indicate alignment marks of the optical mask and the substrate. It is unclear as to which alignment mark is being referred.

The remaining claims are rejected for depending from the above rejected claims.

For the purposes of patentability, the claims will be interpreted as best understood by Examiner.

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Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the article **Im et al.** "Single-crystal Si films for thin-film transistor devices" Applied Physics Letters 70(25) 23 June 1997, pp. 3434-3436 (the article provided by Applicant) in view of US 3,712,740 (**Hennings**) and US 5,821,562 (**Makita et al.**).

Im discloses a method for forming a crystalline semiconductor film at a desired position on a substrate comprising,

preparing a substrate having deposited thereon, amorphous (i.e. first property) semiconductor silicon (a-Si);

preparing an optical mask having a pattern thereon and spacing the mask apart from the substrate;

positioning the mask at the desired position;

irradiating the a-Si through the mask pattern to convert the desired exposed regions to polycrystalline and single crystalline (i.e. second property) semiconductor silicon (Figs. 1 and 2 and captions thereunder);

wherein the crystallized silicon film is for the production of thin film transistors TFTs.

(See whole article -- especially the Abstract, paragraph bridging the cols. on p. 3434 and p. 3436, left-hand col., last paragraph.)

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Im does not indicate that the substrate has an alignment mark previously formed thereon and that said alignment mark is used to position the projection area of the optical mask.

However, **Im** states that “the number and location of these [crystallized silicon] regions can be precisely controlled by using an appropriately patterned mask.” (**Im** p. 3435, left-hand col. last sentence of penultimate paragraph.) This indicates that **Im** suggests precisely controlling the location of each of the crystallized regions.

Hennings, teaches a method of aligning/positioning a mask relative to a semiconductor substrate (called “wafer” in **Hennings**), in order to form a pattern on the wafer wherein an alignment mark is formed first on the substrate and a corresponding alignment mark on the optical mask and then the mask is positioned relative to the substrate on the basis of the alignment marks on the substrate and the optical mask. **Hennings** also teaches that the method is beneficially automated. (See col. 3, last paragraph.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form an alignment mark on the substrate **Im** prior to the crystallization process and to use the alignment mark to position the optical mask of **Im** because (1) **Im** suggests precisely controlling the location of each of the crystallized regions and (2) **Hennings** teaches that forming an alignment mark on the substrate enables positioning of the mask relative to the substrate and is also beneficially automated to simplify the process. Additionally one of ordinary skill would be especially motivated to use an alignment mark on the substrate to position the optical mask of **Im** so that each of the TFTs can be precisely located on the substrate, as is always done in semiconductor manufacture. Transistors are never randomly positioned on a substrate, but have

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their locations precisely planned, as evidenced by the use of lithographic mask sets used to manufacture semiconductor devices on a substrate.

Then the only difference is that **Im** does not indicate that an insulation film is formed on both the crystalline silicon and a-Si (i.e. the first property semiconductor film and the second property semiconductor film). Regarding claim 8, **Im** also does not indicate that the silicon film is patterned to form crystalline silicon islands. However, **Im** does indicate that the crystallized silicon film --especially the single crystal region-- is used to form a TFT which suggests to one of ordinary skill that additional processing to form the TFT will be necessary.

Makita teaches a method of forming a TFT by blanket depositing an amorphous silicon film **402** (Fig. 10B), and then forming an insulation film **413** (Fig. 10J) over the both the first property and the second property silicon films **402**, and **412** to serve as a gate dielectric (Fig. 10K). (See Figs. 10A to 10O and associated text beginning at col. 22, line 30).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to blanket deposit the insulation film of **Makita** over both the a-Si and crystallized silicon of **Im** in order to form the gate dielectric of the TFTs and the alignment marks used to position the rest of the layer, as taught to be beneficial in **Makita**. The patterning to form islands is standard in the art for TFT fabrication as shown in **Makita** and is an obvious modification to **Im** because **Im** teaches that the single crystal silicon region is the best for forming a TFT.

Regarding claims 3, 4, 6, and 10 the prior art of **Im** in view of **Hennings**, as explained above, discloses each of the claimed features except for indicating that the alignment mark pattern on the optical mask forms an alignment mark on the substrate, wherein the alignment

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mark is discernable due to a difference in the optical characteristic difference between the first-property semiconductor film and the second-property semiconductor film.

Makita teaches a method of forming an alignment mark, which is used for a later positioning process (col. 27, lines 36-38), wherein the alignment mark on the substrate is formed from an alignment mark pattern on a mask, and is discernable based upon the different properties of the semiconductor films (col. 26, line 23 to col. 27, line 38; Figs. 12A-12T).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the alignment mark of **Makita** as the alignment mark of **Hennings** because **Hennings** indicates that any alignment feature will work and because **Makita** teaches that the process of forming the alignment mark while also crystallizing the amorphous silicon to form active regions for TFTs, simplifies the processing by reducing the number of process steps since the alignment mark formation and the crystallization are carried out substantially simultaneously.

Response to Arguments

7. Applicant's arguments with respect to all pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. This action is made **non-final** to allow Applicant to respond to the new ground of rejection.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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JP 5-21343 (**Kitakado**), like **Im**, teaches a method of crystallizing selected regions of an amorphous silicon film on an insulating substrate to form TFTs in selected locations. **Kitakado** teaches that it is especially beneficial to form an alignment mark **8** on the substrate **1** before forming the amorphous silicon film and also teaches that the alignment mark is used to position the laser beam for irradiation. (Abstract; paragraphs [0006]-[0008].)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Erik Kielin
April 12, 2003